S-band Transmitter

DATASHEET

ISIS-TXS2-DSH-0001, version 2.2

S-Band Transmitter

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Applications

CubeSat TT&C
CubeSat RF Payloads

General description

The ISIS S-band Transmitter is a CubeSat compatible transmitter designed to meet the needs of high data-rate downlinks of up to 4.3 Mbps (usable information bit-rate at CCSDS TM Transfer Frame level) as well as low data-rate TT&C. The S-band transmitter is flexible, implementing CCSDS as data link layer protocol and allowing in-flight configuration of data-rate, modulation scheme, frequency, and RF output power.

Flight heritage and quality assurance

- IPC-A-610 Class 3 assembly

Product features

- Operates in the 2200-2290 MHz EESS/SRS/SOS allocation
- CCSDS compliant channel coding ensures compatibility with many off-the-shelf demodulators as well as various groundstation networks
- Compatibility with the following demodulators has been verified:
    - Zodiac CORTEX CRT
    - Teledyne Qubeflex
    - Amergint satTRAC
    - RT Logic / KRATOS quantumGND
    - Antwerp Space Omnisat LT
- Compatibility with the following groundstation networks has been verified:
    - KSAT-lite
    - LEAF Space
- Strong Forward Error Correction (FEC) to maximize link throughput
- No need for data pre-processing: all channel coding is performed inside the transmitter
- Up to 4.3 Mbit/s useful datarate (at CCSDS TM Transfer Frame level)
- In-flight configurable RF parameters (Frequency, data-rate, RF power, FEC parameters) – allows to optimize throughput during a satellite overpass
- Data interfaces: LVDS (payload data), I^2C (housekeeping)
- Safety watchdog
- Adjustable RF output power
- Power control loop to keep RF output power constant over varying operating conditions
- On board diplexer to minimize out-of-band emissions and allow optional connection to receiver for full duplex system

Ordering information

Please contact sales@isispace.nl for ordering information

Block Diagram

TXS is based on a MicroSemi SmartFusion2 SoC. A separate supervisor MCU takes care of power switching, telemetry gathering and watchdog functionality. An LVDS interface is provided for high speed payload data, although (low speed) data to be transmitted can also be routed via the I²C bus.

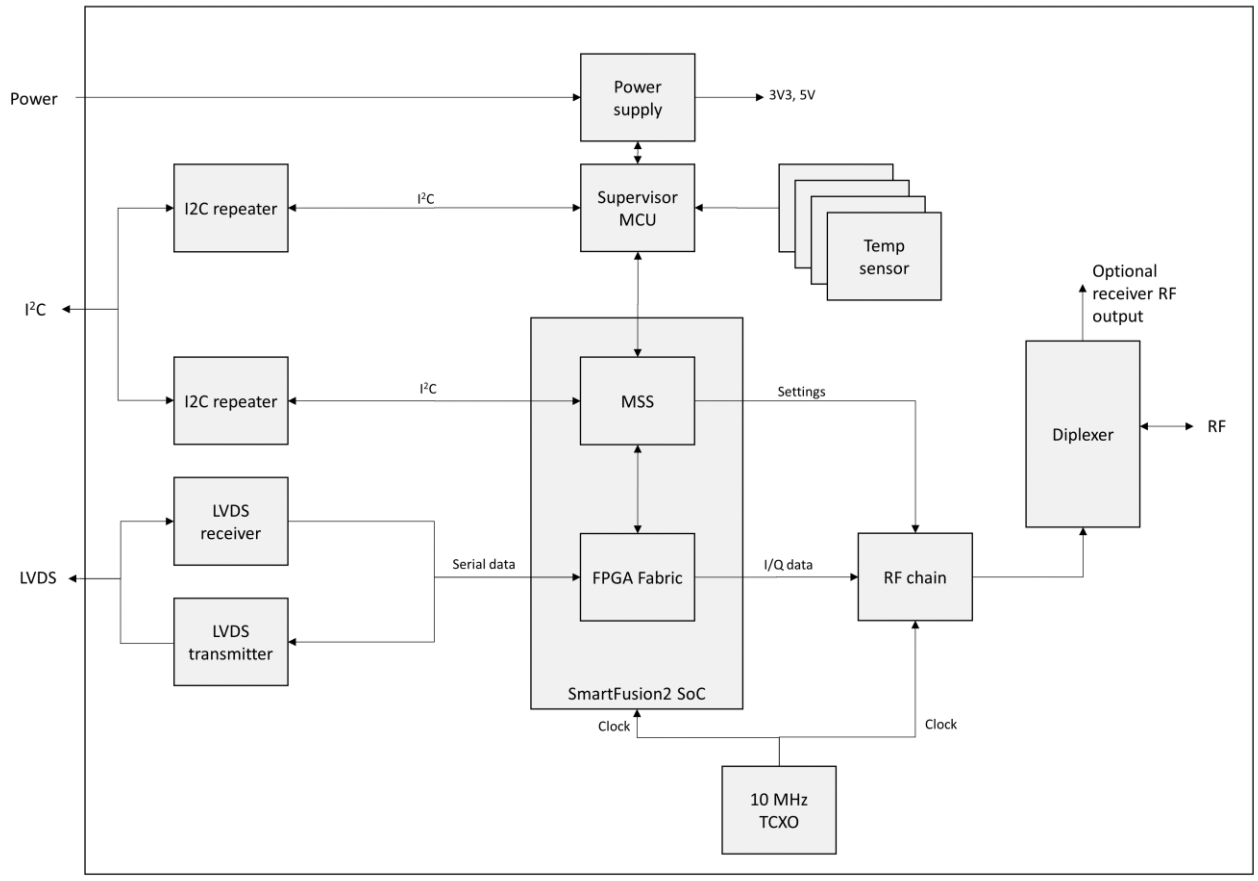

Figure 1 TXS high level block diagram

Specifications

Table 1 TXS Key Specifications

Parameter	Typical Value
Frequency range	2200 – 2290 MHz
Frequency step size	1 kHz
Frequency stability	+/-0.28 ppm
RF output power	27 to 31 dBm (settable) ± 1 dB, up to 33 dBm max.
Spurious emissions	Less than -60 dBc
Transmitted data rate (on-air)	up to 10 Mbit/s (5 Msym/s, OQPSK)
Useful information bitrate	up to 4.3 Mbit/s (at TM transfer frame level)
Supported symbol rates	0.15625, 0.3125, 0.625, 1.25, 2.5, 5 Msym/s selectable
Modulation scheme	Suppressed carrier: BPSK, OQPSK selectable as per CCSDS 401.0-B

Parameter	Typical Value
Pulse shaping filter	Root raised cosine Nyquist pulseshaping as per CCSDS 413.0-G. Roll-off: 0.35 / 0.5 selectable
Forward Error Correction	Convolutional (K=7, ½) as per CCSDS 131.0-B
	Reed Solomon (223, 255) as per CCSDS 131.0-B
Pseudorandomization	Pseudorandomization as per CCSDS 131.0-B
Synchronization	32 bit Attached Sync Marker as per CCSDS 131.0-B
Power consumption	13 W (for 33 dBm RF output power)
DC supply voltage	7 to 20 V
Payload data interface	LVDS
Housekeeping data interface	I2C
Dimensions	98.8 x 93.3 x 14.5 mm
Mass	132 g
Operating temperature	-40 to +70 °C

Electrical Characteristics

Table 2 Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power supply						
DC supply voltage	V_{cc}		7		20	V
DC power consumption	P_{DC}	Mode: Supervisor on		0.08	0.1	W
DC power consumption	P_{DC}	Mode: TX standby		1.5	1.6	W
DC power consumption at rated output power	P_{DC}	Mode: TX on P_{RF} = 33 dBm, Vcc = 16.0 V		13	14	W
RF						
RF output power	P_{RF}	f_{TX} = 2245 MHz, Vcc = 16.0 V	30	31	33	dBm
RF output power stability	ΔP_{RF_T}	-25° C ≤ T_{amb} ≤ 55 ° C		1	2	dB
RF output power stability	ΔP_{RF_f}	2200 MHz ≤ f_{TX} ≤ 2290 MHz		1.5	2	dB
Spurious suppression	N/A	P_{RF} = 33 dBm			-60	dBc
Transmit center frequency	f_{TX}		2200		2290	MHz
Frequency stability	Δf				±0.28	ppm
I^2C interface[1, 2]						
Bus logic low-level input voltage	V_{IL}		0		1.0	V
Bus logic low-level output voltage	V_{OL}		0.47		0.6	V
Bus logic high-level voltage	V_{OH}		2.3		3.3	V
LVDS Outputs[3]						
Differential output voltage	V_{OD}		250	310	450	mV
Offset voltage	V_{OS}		1.125	1.17	1.375	V
Output high voltage	V_{OH}			1.33	1.6	
Output low voltage	V_{OL}		0.90	1.02		V
LVDS Inputs[4]						
Differential input high threshold	V_{TH}	V_{cm} = 1.2 V, 0.05 V, 2.95 V		-35	0	mV
Differential input low threshold	V_{LH}	V_{cm} = 1.2 V, 0.05 V, 2.95 V	-100	-35		mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Common-mode voltage range	V_{CMR}	V_{ID} = 200 mV p-p	0.1		2.3	V
Input current	I_{IN}	V_{IN} = 2.8 V	-10	±5	+10	µA
	I_{IN}	V_{IN} = 0 V	-10	±1	+10	µA
LVDS input termination resistance	R_T			100		Ohm

1. I^2C repeater IC type: PCA9517A
2. The PCA9517A buffers on the TXS are powered by 3.3 V, therefore a nominal bus logic high voltage of 3.3 V is supported
3. LVDS Receiver IC type: ADN4668
4. LVDS Transmitter IC type: ADN4667
5. RF output power over frequency varies per unit due to diplexer frequency response. Refer to the typical performance graphs for typical output power performance versus frequency.

Absolute Maximum Ratings

Stresses at or above the absolute maximum ratings in Table 3 may cause permanent damage to the product. Operation at or beyond the maximum operating ratings may affect product reliability.

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage	Vcc	6	26	V
Operating temperature range	T_{amb}	-20	70	°C
Storage temperature range	$T_{storage}$	-40	85	°C
Voltage on I^2C pins	V_{I2C}	-0.5	7	V
I^2C pull up resistor value	R_{pu}	1.2		kOhm
LVDS input pin voltage	V_{IN_LVDS}	-0.3	3.6	V
LVDS output pin voltage	V_{OUT_LVDS}	-0.3	3.6	V
GPIO input voltage, any GPIO pin	V_{IN_GPIO}	-0.3	3.6	V

Typical Performance Graphs

Conditions: T_{amb} = 25 ° C, V_{cc} = 16.0V unless otherwise stated

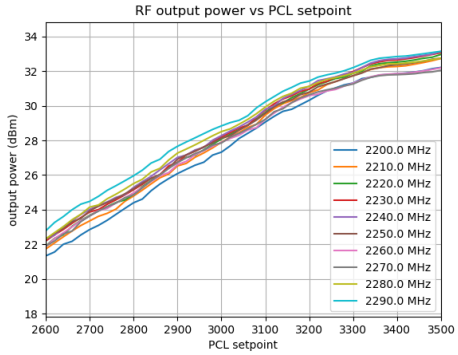

Figure 2 RF output power vs power control loop setpoint for various frequencies (closed loop)

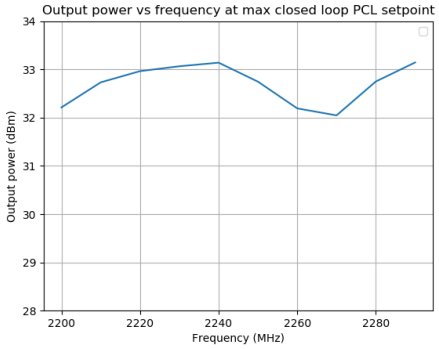

Figure 3 RF output power vs frequency at max closed loop PCL setpoint

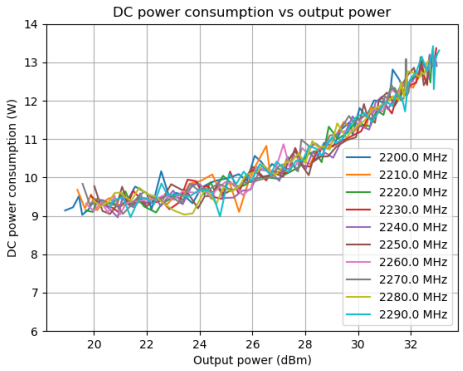

Figure 4 DC power consumption vs RF output power

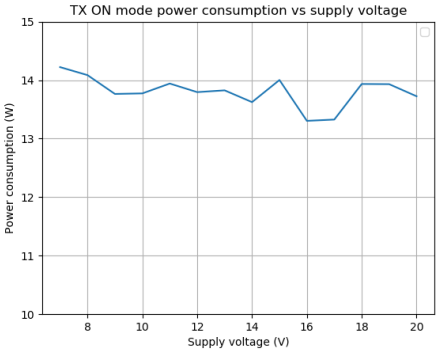

Figure 5 TX ON mode DC power consumption vs supply voltage

Typical link budget

Table 4 provides a typical link budget achieved with TXS to a small groundstation (1.9 m diameter). With larger groundstation G/T, larger usable datarates can be supported at 5 degrees elevation.

Table 4 Typical TXS link budget

Parameter	Value	Unit	Rationale
Frequency	2245.0	MHz	2200-2290 MHz SOS / EESS / SRS space-to-Earth allocation
Satellite transmitter power	0.0	dBW	1W / 30 dBm
Satellite TX losses	1.0	dB	Assumption
Satellite antenna gain	0.0	dBi	Typical patch antenna gain for 5 deg elevation and Nadir pointing satellite
Satellite EIRP	-1.0	dBW	
Satellite pointing loss	0.5	dB	Assumption
Orbital altitude	600000.0	m	Typical LEO orbit
Elevation angle	5	deg	Minimum elevation for communication
Range	2329031.4	m	
Path loss	167.0	dB	
Atmospheric losses	0.5	dB	ITU-R P.676-12

Parameter	Value	Unit	Rationale
Ionospheric losses	0.1	dB	ITU-R P.531-14
Polarization losses	0.0	dB	No polarization mismatch assumed
Earth station pointing loss	1.0	dB	Assumption
Earth station figure of merit	9.0	dB/K	Small S-band station figure of merit (1.9 m diameter antenna)
Channel symbol rate	1250000.0	sym/s	1.25 Msym/sec
Code rate	0.430502	-	CCSDS RS (255, 223) + conv R = 1/2
Information bitrate	538128	bit/s	1.25 Msym/sec OQPSK, RS (255, 223) + conv R = 1/2, interleaving depth = 1
Information bitrate	57.3	dBHz	In dBHz
Implementation loss	2.0	dB	Pessimistic assumption for a typical demodulator
Eb/N0	10.2	dB	
Required Eb/N0	2.4	dB	OQPSK, RS(255, 2223) + C(7, 1/2) for a BER 1E-5
Link margin	**5.8**	dB	

Note: In the above table, losses are denoted by a positive number.

Physical Layout

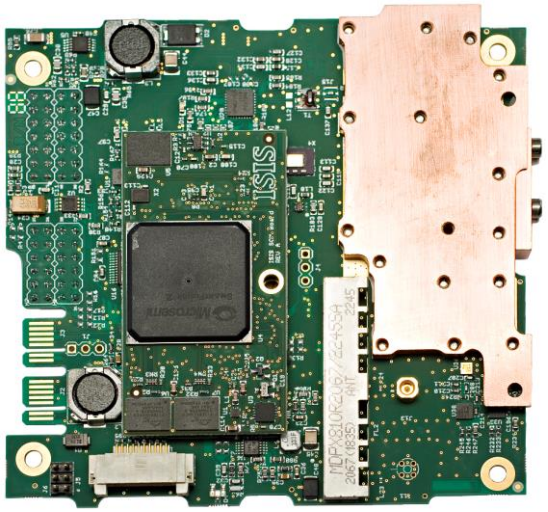

Figure 6 Top view

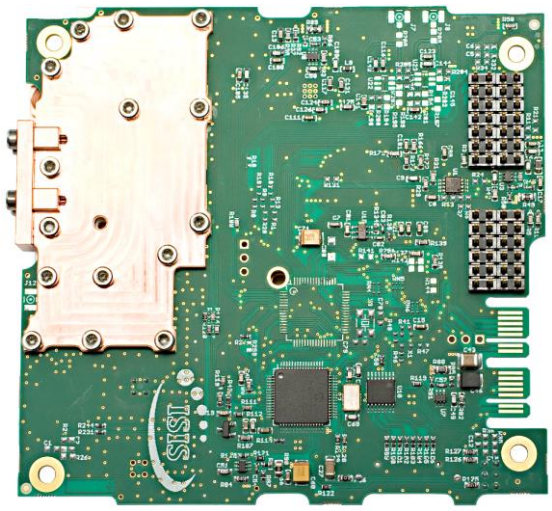

Figure 7 Bottom view

Mechanical outline

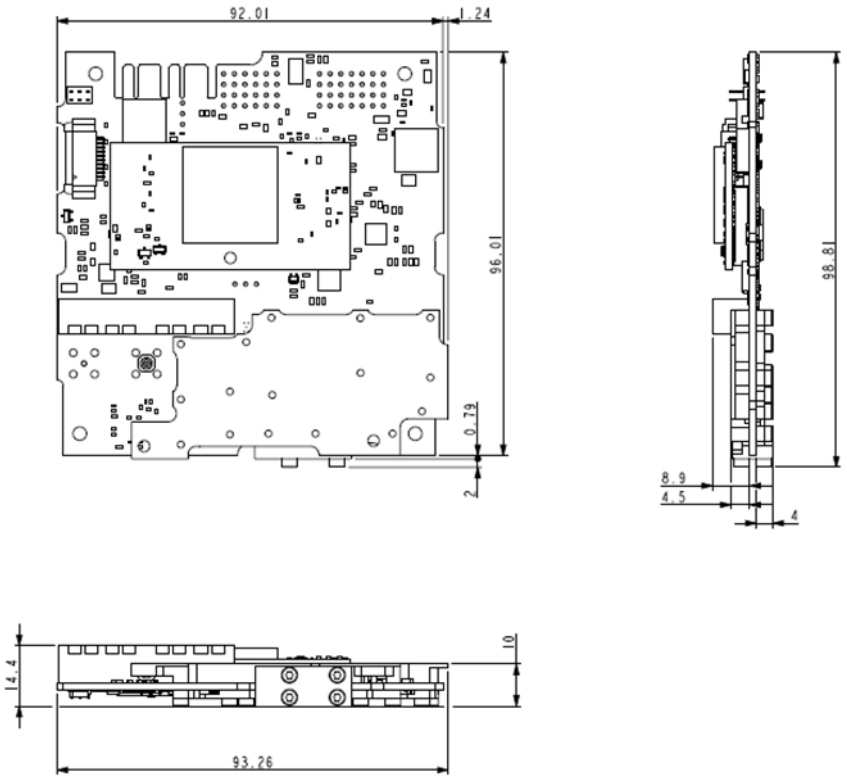

Figure 8 Mechanical outline[1]

Detailed interface information and CAD models of the entire TXS may be delivered on request.

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[1] This mechanical outline drawing does not contain the CSKB-lite connector, since a number of options for this connector are available. Contact ISIS for details.